ACORN KEYBOARD

UNIT DESCRIPTION

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Written and Produced for Acorn Computers Limited by Arch Technical Publications Limited,
St. Lukes House, 5, Walsworth Road, Hitchin, Herts.

1. INTRODUCTION

The Acorn Keyboard provides a 62-key mechanism (Figure 1) using a QWERTY format. The keyboard is supplied in an injection moulded plastic case, and can be connected directly to a dedicated port on the Acorn 6502A CPU Board using a 20-way ribbon cable. Depressed key identity is transmitted to the CPU in 7 bit ASCII code.

Four special function keys provide the following facilities:

- ↑↓, *referred to as the Caps key:* This key functions as a shift key for alphabetic characters only so that only upper case letters are produced, as required when working in languages such as BASIC.
- *REPEAT:* The output lines always carry the code for the last key that was pressed, even if the key has been released. The REPEAT key gives repeated codes for that key to the CPU. An auto repeat feature starts the repeat circuit automatically if a key is held down for longer than 0.5 seconds.
- *BREAK:* This key provides a system reset function.
- ⇄, *referred to as the Blank key:* This key is undefined and can be user programmed via the CPU port.

Two other keys, CTRL (Control) and SHIFT, change the character set produced by the keyboard encoder circuit to give ASCII control characters and upper/ lower case selection respectively.

Three LED indicators on the keyboard provide an indication of Power On, Caps Lock mode and Shift Lock mode.

An optional timer circuit provides a Power-on Reset function.

1.1 PRINCIPLES OF OPERATION

A block diagram of the Acorn Keyboard is given on Figure 2.

The keyboard encoder device is capable of encoding up to 112 keys on a 16 x 8 matrix. It detects a depressed key and outputs a 10 bit code, representing the identity of the depressed key, and a flag signal for the duration of the key depression. Further circuits on the keyboard reformat the 10 bit code into an ASCII, 7 bit code. The key depressed flag signal is fed through a repeat key code circuit before being added to the seven ASCII data bits to form an 8 bit key data byte.

The key data byte in Acorn Systems is fed to Port A on the CPU Board. This port is periodically polled and if the flag bit (NSTROBE) is set, the key code is read. However, the key code remains valid on the port until reset by the next key depression. Thus, it is only necessary to set the NSTROBE signal again (by means of the Repeat Circuit) to obtain the Repeat facility.

The Caps key forms part of the reformatting circuit, automatically amending the ASCII code to ensure that, in the Caps mode any lower case alphabetic codes are converted to upper case.

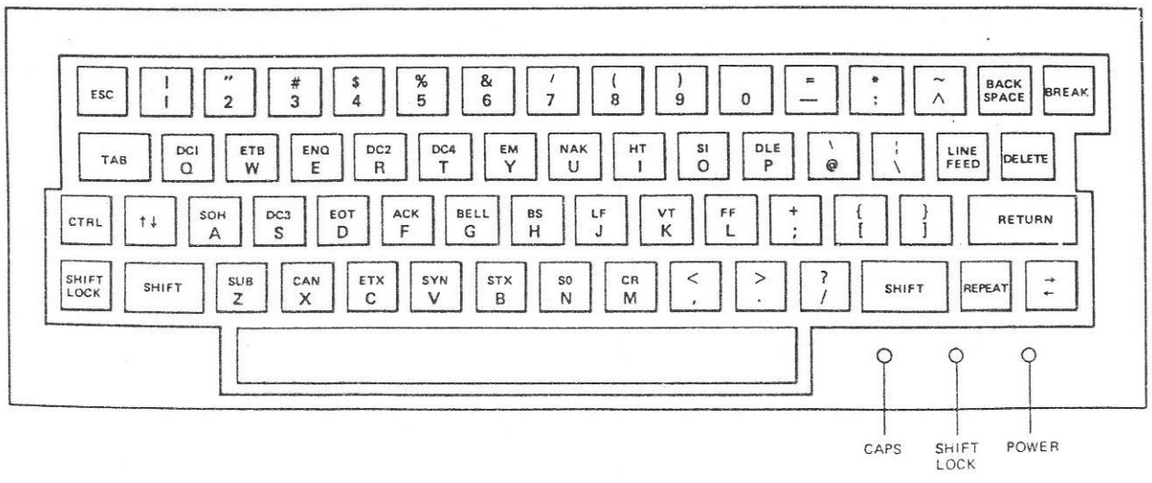

Figure 1. Keypad

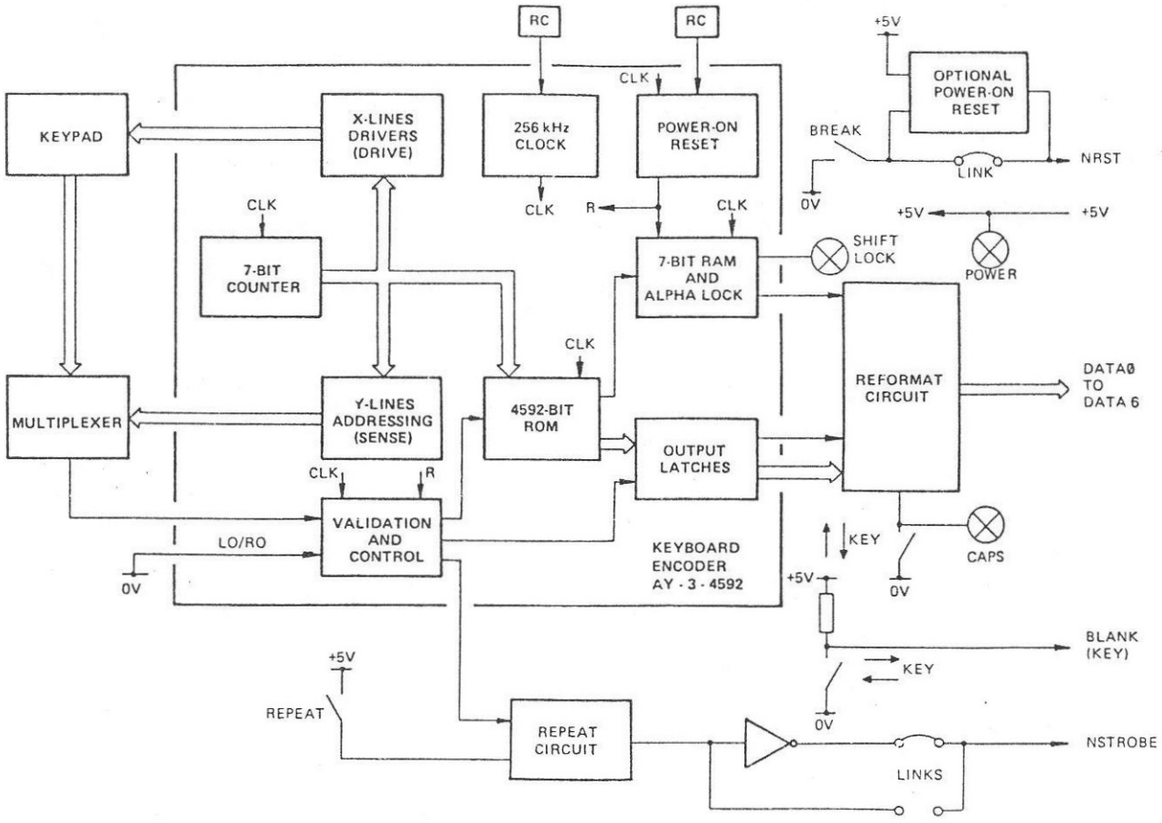

Figure 2. Keyboard Block Diagram

The BREAK key forms part of the optional Reset Circuit when fitted. The Blank to 10 port bit user programmable key is connected directly to Port A on the CPU Board.

1:2 LEADING PARTICULARS

1.2.1 Mechanical

Construction :Special printed circuit board carrying 62 keys.

Housing :Injection moulded ABS case.

Size :PCB and keypad: 355mm x 150mm, overall height 30mm.

Case: 380mm x 240mm, overall height 60mm.

1.2.2 Power Supplies

+5V at 100mA maximum.

1.2.3 Connections

Output Signals and power supplies : 20-way flying lead ribbon header-

Alternatively, connection may be made to the 20-way PCB edge connector.

Output Signals are TTL compatible : Logic '0' = 0V to +0.4V
Logic '1' = +2.4V to +5.25V.

2. CIRCUIT DESCRIPTION

The circuit diagram for the Acorn Keyboard is at the end of this section.

2.1 ENCODER

The keys are connected to the keyboard encoder device, IC1 on a 13 x 8 matrix. Scanning of the matrix is performed by the encoder in conjunction with an

external 3 to 8 multiplexer, IC2. The encoder provides a 3 bit binary address (YA, YB and YC) which is used cyclically to scan each of the eight possible sense lines (Y lines). The drive lines (X lines) are cyclically pulsed low by the encoder. If a key is depressed, the pulse is coupled from the drive line to the sense line at that key's matrix crosspoint and via IC2 to the NMATIN input of the encoder.

Each matrix crosspoint is given a unique binary code that is determined by internal scan counters. This code is loaded into a 7 bit latch and compared with the matrix code generated by the depressed key on the next scan. If the two codes match, a valid key depression, the matrix code is used to address the 4592 bit, ROM which holds the encoder output codes. The output code is loaded into the output holding register (output pins D1 to D10). At the same time, the code match generates the Any Key Depressed flag (AKD).

If a second key is depressed before the first key has been released, the AKD output goes low (inactive) for two clock cycles (8µs) and the code for the second key is latched onto the output lines.

A two key rollover facility is provided by connecting pin 13 (LO/RO) to 0V. This modifies the foregoing key detection action to encode the second key depression when two keys are depressed almost simultaneously (first key miskeyed) within the space of one matrix scan. When the matrix crosspoint codes are compared, a mismatch occurs and the code generated at the second scan is assumed to be the valid code.

Timing for the encoder is provided by an internal clock generator whose frequency is set to 256kHz by the external components R1 and C1. This results in an effective (double) keyboard scantime of 8ms. The keyboard inhibit facility (pin 12, KBINH) is not used.

At Power On, pin 37 (POR) is held low for approximately 100ms until C2 charges through R2. This action clears all the internal registers and bistables. The SHIFT LOCK key, when depressed, produces an additional output, SLI (pin 34). This is used to light the SHIFT LOCK indicator via inverter, IC/8.

Circuits within the encoder device guard against errors due to simultaneous depression of two or more keys and provide key debouncing.

2.2 REFORMAT CIRCUIT

This circuit takes eight bits (D1 to D5, D7 and D6 or D9) from the 10 bit output code and reformats them into a 7 bit ASCII/ISO/CCITT No. 5 Telegraphy/Data Transmission code.

Output code bits D1 to D5 and D7 are inverted by the hex inverters IC5 and IC6/6 to produce the ASCII code bits DATA0 to DATA4 and DATA6 respectively.

In the Caps Lock mode (Caps key depressed), the low input to IC4 pin 12 from the Caps key inhibits IC4/11 and thus output code data bit D6 (alphabetic lower case indicator bit). The same low input is inverted by IC4/6, enabling IC4/8 and the feeding of output code data bit D9 (alphabetic upper case indicator bit) via IC4/8 and IC4/3 (double inversion) to the output inverter IC5/12 as DATA5 bit. The Caps key depressed also lights the CAPS LOCK indicator (LED D2) via resistor R8.

in all other modes, the inputs to IC4/6 and pin 12 of IC4 are pulled high via R8 and D2. This inhibits output code bit D9 via IC4/8 and enables output code bit D6 via IC4/11 and IC4/3 (double inversion) and the output inverter IC5/12 (DATA5).

2.3 REPEAT CIRCUIT

This circuit (IC3) provides two Repeat Last Key facilities. It causes the key depressed coded to be retransmitted at a rate of 10Hz if the depressed key is held down for longer than 0.5s or if the REPEAT key is operated after the release of the depressed key and before operation of another key.

Initially, signal AKD from IC1 is low, C3 is discharged to AKD though D1, and the input to pin 2 of IC3 is high.

When a key is depressed, AKD goes high, is inverted by IC3/3, and fed via IC6/2 and IC6/4 (double inversion) to the output pin 18 (NSTROBE). For applications requiring a positive strobe, the printed circuit track from IC6 pin 4 to output pin 18 should be cut and a link made between IC6 pin 2 to output pin 18.

While a key is depressed, capacitor C3 begins to change towards AKD through R6 and R3. This is ineffectual unless the key is held down for longer than 0.5s, the time constant of C3 and R6.

If a key is held down for longer than 0.5s,. C3 charges fully and the pin 8 input to IC3 goes high. The pin 9 input to IC3 is already high due to the action of C4.

R5/VR1, and IC3/4 and the output of IC3/10 goes low inhibiting IC3/3, and setting NSTROBE high. Since IC3/10 output is low and IC3/3 output is high, C3 reverse charges (in 100ms), the output of IC3/4 goes low enabling IC3/3 again via IC3/10 and resetting NSTROBE low. This oscillatory action of C4, IC3/4 and IC3 at 10Hz (100ms) continues until the depressed key is released.

Depression of the REPEAT key immediately charges C3, repeating the foregoing operation without the initial 0.5s delay required to charge C3.

2.4 SYSTEM RESET

The System Reset pulse (NRST) is generated by operation of the BREAK key which connects the NRST output pin to 0V. The link between the BREAK key and the NRST output pin must be connected for this type of operation.

Alternatively, the NRST pulse can be generated at power on by the optional timer circuit of IC7 and at other times by the action of the BREAK key in conjunction with the timer. The link is disconnected for this type of operation.

The timer is connected in the monostable mode with R12 and C9 providing the timing, and the BREAK key connected to the trigger input (pin 2).

At power on, the trigger input is low (C8 discharged), setting the internal circuits so that the output (pin 3) is high inverted by IC6/10 to produce NRST low) and allowing C9 to charge through R12. After approximately 100ms C9 (andC8) will have charged, resetting the internal circuits to give a low output and discharging C9. Thus the NRST line is held low for 100ms to provide the System Reset at power on.

When the BREAK key is depressed to generate a user controlled system Reset, C8 is discharged, and the trigger input goes low. This results in the generation of the 100ms NRST pulse as described above.

2.5 USER PROGRAMMABLE KEY

The Blank user programmable key is connected directly to pin 5 of the edge connector. With the key in the OFF state, this pin is pulled high by resistor R7.

3. SOFTWARE PARAMETERS

The following table defines the ASCII 7 bit codes produced by depressed keys under the five basic modes of operation:

Normal	Unshifted (lower case) character set.
Shifted	Upper case character set.
Control	Control codes.
Shift/Control	The character set and control codes produced when the SHIFT and CONTROL keys are operated.
Caps Lock	The numeric/upper case alphabetic and symbol character set produced by operation of the Caps key.

4. KEYBOARD CONNECTIONS

The Acorn Keyboard outgoing signals and incoming power supply are connected via a 20-way header cable. The remote end of this cable is identified as CPU Pin in the following list.

Keyboard Pin	CPU Pin	Circuit Mnemonic	Meaning	I/O
1	11	0V	Earth	–
2		–		–
3		–		–
4		–		–
5	1	'BLANK'	Customer/Software specified	O
6		--		–
7		–		–
8		–		–
9		–		–
10		–		–
11	10	DATA0		O
12	12	DATA1		O
13	14	DATA2	Key Identity	O
14	16	DATA3	7 bit ASCII	O
15	18	DATA4	Code	O
16	20	DATA5		O
17	19	DATA6		O
18	17	NSTROBE	Key Operation flag	O
19	15	NRST	System Reset	O
20	13	+5V	+5V Line	1

NORMAL		SHIFT		CONTROL		SHIFT & CONTROL		TTY CAPS	
CHARACTER	HEX	CHARACTER	HEX	CHARACTER	HEX	CHARACTER	HEX	CHARACTER	HEX
TAB	Ø9	TAB	Ø9	TAB	Ø9	TAB	Ø9	TAB	Ø9
LINE FEED	ØA	LINE FEED	ØA	LINE FEED	ØA	LINE FEED	ØA	LINE FEED	ØA
RETURN	ØD	RETURN	ØD	RETURN	ØD	RETURN	ØD	RETURN	ØD
ESC	1B	ESC	1B	ESC	1B	ESC	1B	ESC	1B
SPACE BAR	2Ø	SPACE BAR	2Ø	SPACE BAR	2Ø	SPACE BAR	2Ø	SPACE BAR	2Ø
0	3Ø	0	3Ø	0	3Ø	0	3Ø	0	3Ø
1	31	!	21	1	31	!	21	1	31
2	32	"	22	2	32	"	22	2	32
3	33	#	23	3	33	#	23	3	33
4	34	$	24	4	34	$	24	4	34
5	35	%	25	5	35	%	25	5	35
6	36	&	26	6	36	&	26	6	36
7	37	'	27	7	37	'	27	7	37
8	38	(	28	8	38	(	28	8	38
9	39	)	29	9	39	)	29	9	39
a	61	A	41	SOH	Ø1	SOH	Ø1	A	41
b	62	B	42	STX	Ø2	STX	Ø2	B	42
c	63	C	43	ETX	Ø3	ETX	Ø3	C	43
d	64	D	44	EOT	Ø4	EOT	Ø4	D	44
e	65	E	45	ENQ	Ø5	ENQ	Ø5	E	45
f	66	F	46	ACK	Ø6	ACK	Ø6	F	46
g	67	G	47	BELL	Ø7	BELL	Ø7	G	47
h	68	H	48	BS	Ø8	BS	Ø8	H	48
i	69	I	49	HT	Ø9	HT	Ø9	I	49
j	6A	J	4A	LF	ØA	LF	ØA	J	4A
k	6B	K	4B	VT	ØB	VT	ØB	K	4B
l	6C	L	4C	FF	ØC	FF	ØC	L	4C
m	6D	M	4D	CR	ØD	CR	ØD	M	4D
n	6E	N	4E	S0	ØE	S0	ØE	N	4E
o	6F	O	4F	S1	ØF	S1	ØF	O	4F
p	7Ø	P	5Ø	DLE	1Ø	DLE	1Ø	P	5Ø
q	71	Q	51	DC1	11	DC1	11	Q	51
r	72	R	52	DC2	12	DC2	12	R	52
s	73	S	53	DC3	13	DC3	13	S	53
t	74	T	54	DC4	14	DC4	14	T	54
u	75	U	55	NAK	15	NAK	15	U	55
v	76	V	56	SYN	16	SYN	16	V	56
w	77	W	57	ETB	17	ETB	17	W	57
x	78	X	58	CAN	18	CAN	18	X	58
y	79	Y	59	EM	19	EM	19	Y	59
z	7A	Z	5A	SUB	1A	SUB	1A	Z	5A
,	2C	<	3C	,	2C	<	3C	,	2C
- (1)	2D	_ (1)	5F	US (1)	1F	_ (1)	5F	- (1)	2D
.	2E	>	3E	.	2E	>	3E	.	2E
/	2F	?	3F	/	2F	?	3F	/	2F
:	3A	*	2A	:	3A	*	2A	:	3A
;	3B	+	2B	;	3B	+	2B	;	3B
@	4Ø	\	5C	NUL	ØØ	NUL	ØØ	@	4Ø
[	5B	{	7B	ESC	1B	ESC	1B	[	5B
\	5C	:	7C	FS	1C	FS	1C	\	5C
]	5D	}	7D	GS	1D	GS	1D	]	5D
^	5E	~	7E	RS	1E	RS	1E	^	5E
- (2)	2D	= (2)	3D	_ (2)	2D	= (2)	3D	- (2)	2D
DELETE	7F	DELETE	7F	DELETE	7F	DELETE	7F	DELETE	7F

NOTES: 1. BACKSPACE key produces - (minus), _ (underline), and US (Unit separation).

2. = key produces - (minus), and = (equals). (2

Table 1. Key Codes

5. PARTS LIST

5.1 MECHANICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
	Printed Circuit Board 200,013		1	
	Keyboard, Hi-Tech 873-10492		1	
	Ribbon cable, 20-way		2 ft	
	IDC Socket, 20-way		1	
	Strain relief for above		1	
	Case assembly		1	

5.2 ELECTRICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
C1	Capacitor, disc ceramic	1nF	1	
C2	Capacitor, disc ceramic	100n F	1	
C3	Capacitor, tantalum	470nF	1	
C4...C6	Capacitor, disc ceramic	47nF	3	
C7	Capacitor, electrolytic	22µF	1	
D1	Diode	1N4148	1	
D2...D4	Light emitting diode	TIL 228, Red	3	
IC1	integrated circuit	AY-3-4592	1	
IC2	Integrated circuit	CD4051B	1	
IC3	Integrated circuit	CD4093B	1	
IC4	integrated circuit	74 LS00	1	
IC5, IC6	Integrated circuit	74 LS04	2	
R1	Resistor	10K	1	
R2	Resistor	100K	1	
R3	Resistor	10K	1	
R4	Resistor	100K	1	
R5	Resistor	1M	.1	
R6	Resistor,variable	1M	1	
R7	Resistor	4K7	1	
R8... R10	Resistor	270	3	

5.3 POWER—ON RESET OPTION

The following additional components are required to implement the Power-on Reset Option.

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
C8...C10	Capacitor, disc ceramic	100n	3	
IC7	Integrated circuit	555	1	
R11, R12	Resistor	1M	2	

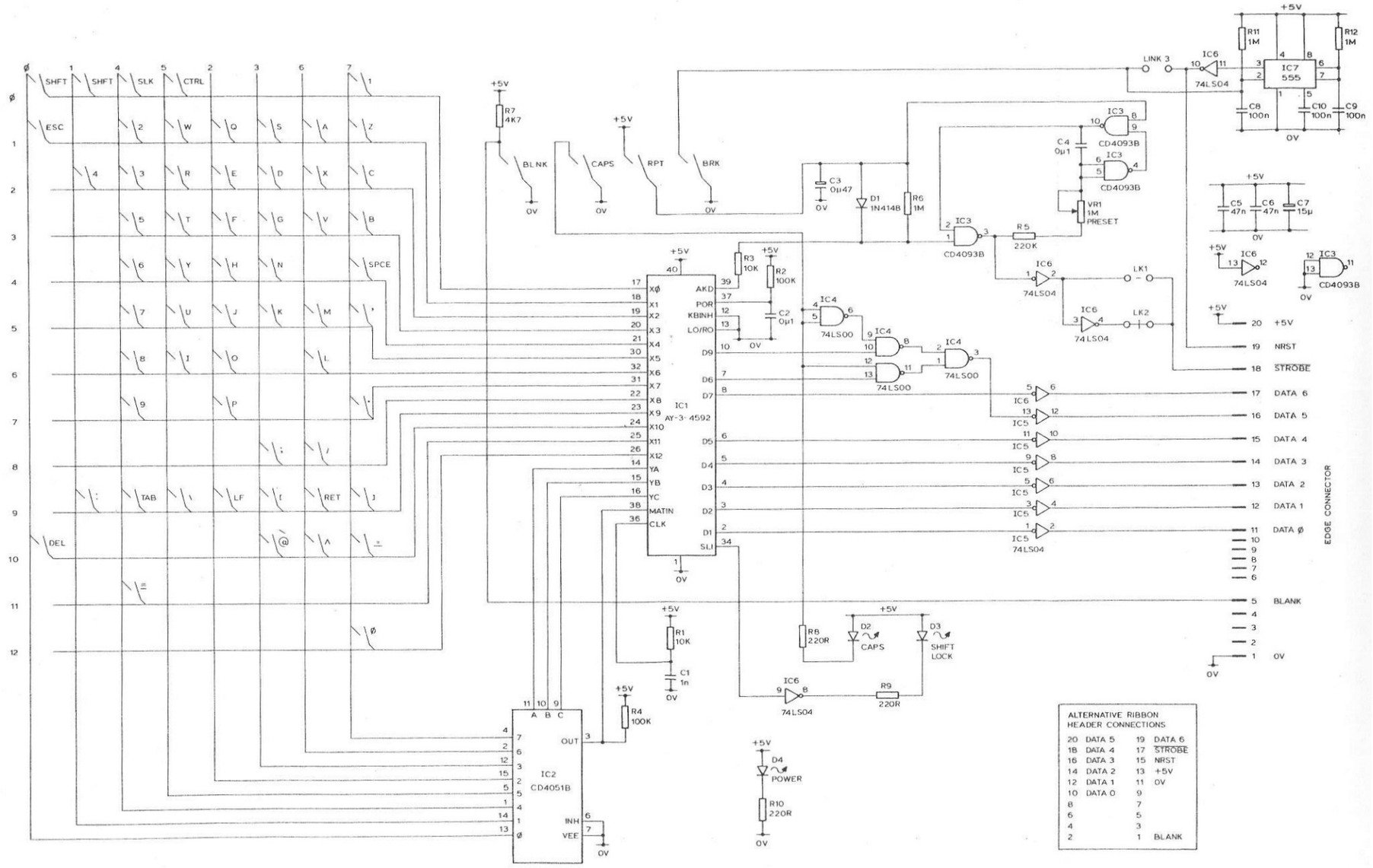

Figure 3. Keyboard Circuit Diagram